In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended): A high voltage device comprising:

a substrate of a first type;

[[a]] first and second [[well]] wells respectively of the first type and a second type in the substrate;

a gate formed on ~~the substrate~~ a junction between the first and second wells, without a field oxide between the gate and the first and second wells;

[[a]]first and second doped ~~region~~ regions both of the second type, respectively formed in the first and second [[well]] wells and both sides of the gate; and

a third doped region of the first type in the first well and adjacent to the first doped region.

2. (original): The high voltage device as claimed in claim 1 further comprising field oxides isolating the high voltage device from other devices on the substrate.

3. (original) The high voltage device as claimed in claim 1, wherein the gate comprises a gate oxide on the substrate, a conducting layer on the gate oxide and spacers on two sides of the gate oxide and conducting layer.

4. (original): The high voltage device as claimed in claim 3 further comprising a fourth lightly doped region of the second type adjacent to the first doped region and beneath one of the spacers.

5. (original): The high voltage device as claimed in claim 1, wherein there is a spacing of the second doped region to the gate.

6. (cancelled).

7. (currently amended): The high voltage device as claimed in claim 1, wherein the first and second types are respectively P and N [[type]] types.

8. (currently amended): The high voltage device as claimed in claim 1, wherein the first and second [[type]] types are respectively N and P [[type]] types and the high voltage device further comprises a N+ buried layer in the substrate and beneath the first and second [[well]] wells.

9. (currently amended): A high voltage device formed on a P substrate comprising:

an HVNMOS comprising:

[[a]] first P and N [[well]] wells in the P substrate;

a first gate formed on ~~the P substrate~~ a junction between the first P and N wells, without a field oxide between the gate and the first P and N wells;

two first N+ doped regions respectively formed in the first P and N [[well]] wells, and both sides of the first gate; and

a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and

a HVPMOS comprising:

an N+ buried layer in the P substrate;

[[a]] second N and P [[well]] wells in the P substrate and above the N+ buried layer;

a second gate formed on ~~the P substrate~~ a junction between the second N and P wells, without a field oxide between the gate and the second P and N wells;

two second P+ doped regions respectively formed in the second N and P [[well]] wells, and both sides of the second gate; and

a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well.

10. (original): The high voltage device as claimed in claim 9 further comprising field oxides isolating the HVPMOS and HVNMOS from other devices on the P substrate.

11. (original): The high voltage device as claimed in claim 9, wherein each of the first and second gates comprise a gate oxide on the P substrate, a conducting layer on the gate oxide and spacers on both sides of the gate oxide and conducting layer.

12. (original): The high voltage device as claimed in claim 11, wherein the HVNMOS further comprises an N lightly doped region adjacent to the first N doped region in the first P well and beneath one of the spacers of the first gate, and the HVPMOS further comprises a P lightly doped region adjacent to the second P doped region in the second N well and beneath one of the spacers of the second gate.

13.(original): The high voltage device as claimed in claim 9, wherein there is spacing of the first N+ doped region in the first N well to the first gate and the second P+ doped region in the second P well to the second gate.

14. (cancelled).

15. (currently amended): A method for manufacturing a high voltage device, comprising the steps of:

providing a substrate of a first type;

forming [[a]] first and second [[well]] wells respectively of the first type and a second type in the substrate;

forming a gate on ~~the substrate~~ a junction between the first and second wells, without a field oxide formed between the gate and the first and second wells;

forming [[a]]first and second doped ~~region~~ regions both of the second type, respectively in the first and second [[well]] wells and both sides of the gate; and

forming a third doped region of the first type in the first well and adjacent to the first doped region.

16. (original): The method as claimed in claim 15 further comprising the step of:

forming field oxides isolating the high voltage device from other devices on the substrate.

17. (original): The method as claimed in claim 15, wherein the gate comprises a gate oxide on the substrate, a conducting layer on the gate oxide and spacers on two sides of the gate oxide and conducting layer.

18. (original): The method as claimed in claim 17 further comprising the step of:

forming a fourth lightly doped region of the second type adjacent to the first doped region and beneath one of the spacers.

19. (original): The method as claimed in claim 15, wherein there is a spacing of the second doped region to the gate.

20. (cancelled).

21. (currently amended): The method as claimed in claim 15, wherein the first and second [[type]] types are respectively P and N [[type]] types.

22. (currently amended): The method as claimed in claim 15, wherein the first and second [[type]] types are respectively N and P [[type]] types and the method further comprises the step of:

forming an N+ buried layer in the substrate and beneath the first and second well.

23. (currently amended): A method for manufacturing a high voltage device comprising the steps of:

providing a P substrate;

forming a HVNMOS on the P substrate by:

forming [[a]] first P and N [[well]] wells in the P substrate;

forming a first gate on ~~the P substrate~~ a junction between the first P and N wells, without a field oxide between the gate and the first P and N wells;

forming two first N+ doped regions respectively in the first P and N [[well]] wells, and both sides of the first gate; and

forming a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and

forming a HVPMOS on the P substrate by:

forming an N+ buried layer in the P substrate;

forming [[a]] second N and P [[well]] wells in the P substrate and above the N+ buried layer;

forming a second gate on ~~the P substrate~~ a junction between the second N and P wells, without a field oxide between the gate and the second P and N wells;

forming two second P+ doped regions respectively in the second N and P [[well]] wells, and both sides of the second gate; and

forming a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well.

24. (original): The method as claimed in claim 23 further comprising the step of:

forming field oxides isolating the HVPMOS and HVNMOS from other devices on the P substrate.

25. (currently amended): The method as claimed in claim 23, wherein each of the first and second [[gate]] gates comprises a gate oxide on the P substrate, a conducting layer on the gate oxide and spacers on both sides of the gate oxide and conducting layer.

26. (original): The method as claimed in claim 25 further comprising the steps of:

forming a N lightly doped region adjacent to the first N doped region in the first P well and beneath one of the spacers of the first gate; and

forming a P lightly doped region adjacent to the second P doped region in the second N well and beneath one of the spacers of the second gate.

27. (original): T The method as claimed in claim 23, wherein there is spacing of the first N+ doped region in the first N well to the first gate and the second P+ doped region in the second P well to the second gate.

28. (cancelled).